REMARKS

On page 2 of the Office Action mailed on June 9, 2009, the drawings were objected to. The Examiner asserts that that the subject matter of claim 9 is not supported by Figure 9 and its associated text in the detailed description of the invention. Applicant refers the Examiner to paragraph [0118] of the published application (US 2004/0169529), which clearly describes the invention as set forth in claim 9. Applicant requests that the Examiner carefully read this paragraph as the Examiner does not appear to understand the invention. For example, the Examiner asserts on page 2 of the Office Action that "the measuring (comparing) of the input signal at node 1004 begins when node 1014 goes to logic '1'." This is incorrect. See, e.g., lines 16-24 of paragraph [0118] of the published application, which states, "At a preselected interval before the measurement begins, but before DataIn begins to change, activate signal (GWSELH) 1014 is asserted to logic HIGH, thereby isolating the input node 1002 of the transistor M162 1008. The DataIn voltage existing just before the measurement is taken is sampled and held as a reference, thereby making the circuit substantially independent of ground or supply voltage references." Thus it can be seen that the measuring of the *input signal* at node 1004 does not begin when node 1014 goes to logic "1," as asserted by the Examiner. Instead, the asserting of the activate signal at node 1014 to logic "1" causes the sampling of node 1004 *before* the input signal is present at node 1004. The Examiner seems to be having a hard time distinguishing between a signal and a node. A given node may have different signals present at said node at different times, and in fact may, at times, have no signal present at all. Once this distinction is understood, it is clear that claim 9 is clearly supported by Figure 9 and its associated text in the detailed description of the invention.

Claims 9 and 10 were also rejected under 35 U.S.C. § 112, ¶ 2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner refers to the objection to the drawings in supporting this rejection. Applicant submits that the claims are definite for the reasons set forth above with respect to the objection to the drawings. The Examiner also asserts that "the voltage present at the input node is the input signal, and thus to recite that the sampling of the voltage at the input node occurs after sampling of the input signal makes no sense." Again, the Examiner seems to be having a

hard time distinguishing between a signal and a node. A given node may have different signals present at said node at different times, and in fact may, at times, have no signal present at all. With the present invention, the asserting of the activate signal at node 1014 to logic "1" causes the sampling of node 1004 *before* the input signal is present at node 1004. Therefore, Applicant submits that the claims particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 9 and 10 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,343,428 ("Pilo"). Applicant submits that Pilo does not anticipate claims 9 and 10. Regarding claim 9, the Examiner asserts that the recited "sampling a voltage present at an input node" reads on the operation of turning on either transmission gate 43 or transmission gate 52. But Pilo does not teach sampling a voltage present at transmission gates 43 or 52 a predetermined interval before measurement of the input signal is initiated, as set forth in claim 9. This is one reason why claim 9 is not anticipated by Pilo.

The Examiner further asserts that the recited "holding the sampled voltage at a reference node as a reference voltage" reads on the operation of storing MUXLAT or MUXLAT* on capacitor 56 or 57. Applicant submits that signals MUXLAT and MUXLAT* are not stored on capacitors 56 and 57 as "reference voltages." The term "reference voltage" is a term of art that is well understood by those of skill in the art of sensing amplifiers as referring to a reference point to which a single-ended input signal is compared. Nodes 101 and 102 of Pilo, which would hold any voltage stored on capacitors 56 and 57, do not function to store a reference voltage of the sense amplifier 20. In fact, the sense amplifier 20 of Pilo is a differential amplifier, as opposed to a single-ended amplifier. The sense amplifier 20 of Pilo senses the difference between complementary data input signals MUXLAT and MUXLAT*, using differential amplifier 25.[1] Because the sense amplifier 20 of Pilo is a *differential* amplifier, it does not make use of a reference voltage at all. The nodes 101 and 102 of Pilo are not reference nodes, but rather are the nodes via which the complementary input signals MUXLAT and MUXLAT* are inputted to

[1] See, e.g., Pilo, et al., US Patent 5,343,428, col. 5, lines 12-16.

the differential amplifier 25, or, alternatively, stored in latch 35.[2] This is further reason that claim 9 is not anticipated by Pilo.

The Examiner further asserts that the recited "sampling the input signal and comparing it to the reference voltage" reads on the operation where signal MUXLAT is compared to MUXLAT* (or vice-versa) after the two signals have passed through the transmission gates. The Examiner is here truncating the claim element at issue and alleging that the truncated portion of the claim element is taught by Pilo. However, the full claim element the Examiner here refers to is "measuring the input signal at the input node by sampling the input signal and comparing it to the reference voltage." The Examiner alleges this reads on the operation where signal MUXLAT is compared to MUXLAT* (or vice-versa) after the two signals have passed through the transmission gates. However, this operation does not take place at the input node (transmission gate 43 or 52 as asserted by the Examiner) as required by the wording of claim 9. That is, the comparing of MUXLAT to MUXLAT* *after the two signals have passed through the transmission gates 43 and 52* does not constitute "measuring the input signal *at the input node* by sampling the input signal and comparing it to the reference voltage" per claim 9. This is yet another reason why claim 9 is not anticipated by Pilo.

In view of the foregoing, Applicant respectfully requests allowance of claim 9 and claim 10 depending therefrom.

[2] *Id.*

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Respectfully submitted,

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